Improving the LDMOS Temperature Compensation Bias Circuit to Optimize Back-Off

Antonis Constantinides, Christos Yiallouras, Christakis Damianou

Abstract—The application of today's semiconductor transistors in high power UHF DVB-T linear amplifiers has evolved significantly by utilizing LDMOS technology. This fact provides engineers with the option to design a single transistor signal amplifier which enables output power and linearity that was unobtainable previously using bipolar junction transistors or later type first generation MOSFETS. The quiescent current stability in terms of thermal variations of the LDMOS guarantees a robust operation in any topology of DVB-T signal amplifiers. Otherwise, progressively uncontrolled heat dissipation enhancement on the LDMOS case can degrade the amplifier's crucial parameters in regards to the gain, linearity and RF stability, resulting in dysfunctional operation or a total destruction of the unit. This paper presents one more sophisticated approach from the traditional biasing circuits used so far in LDMOS DVB-T amplifiers. It utilizes a microprocessor control technology, providing stability in topologies where IDQ must be perfectly accurate.

Keywords-Amplifier, DVB-T, LDMOS, MOSFETS.

I. INTRODUCTION

UPON the innovation of bipolar junction transistor devices in 1947, biasing played a determined role in the performance of linear solid state RF amplifiers, especially when synthesized by complex waveforms. Potential divided resistor networks, zener diode and voltage regulator approaches were the first early stage biasing circuits for bipolar transistors C. BOWICK (2008) [1]. The latest innovation of MOSFET¹ semiconductors has provided superior performance as compared to bipolar junction transistors, and consequently has been popular in UHF² TV amplifiers.

MOSFET amplifiers have been incorporated by a biasing circuit, utilizing a diode semiconductor for temperature compensation purposes and have been demonstrated by semiconductor manufacturers' data sheets like Motorola RF Device Data [2].

Currently, LDMOS³ technology is used exclusively in DVB-T amplifiers as they claim to provide superior linearity and efficiency in OFDM linear applications, A. Ullaf Kashif 2010 [3] where the complexity of the waveform is described

Christos Yiallouras is with the MEDSONIC LTD, Limassol, Cyprus (email: christosyiallouras@gmail.com).

Christakis Damianou is with the Cyprus University Cyprus, Limassol, Cyprus (email: christakis.damianou@cut.ac.cy).

¹ metal–oxide–semiconductor field-effect transistor

 2 Ultra high frequency (UHF) designates the ITU radio frequency range of electromagnetic waves between 300 MHz and 3 GHz

³ laterally diffused metal oxide semiconductor

under:

The DVB-T⁴, OFDM⁵ is a very complex signal, compressed in 2K or 8K DVB-T mode operation, i.e. the 2K mode contains 1705 carriers spaced 4KHz apart while on the other hand, the 8K mode contains 6817 carriers spaced at 1KHz apart [4] and it is illustrated in Fig. 1.



Fig. 1 DVB-T Spectrum

As a result, a reliable thermal stability [5] of the amplifier will sustain linearity and minimize B.E.R⁶ that causes spectral re-growth in the adjacent channel [4]. For example, to settle the proper peak to-average power ratio (PAPR), a DVB-T amplifier must be operated with an average power 'backed off' for achieving the adequate linearity, but at the price of poor efficiency, that causes an excessive amount of heat [6]. Furthermore, high distortion due to thermal instability can also cause a digital pre-distortion to become disabled to compensate. In this regard, it is worth stating that the DVB-T amplifiers enable peaks 20 times higher than their average power. Previous tests, have demonstrated that a DVB-T signal to a crest factor of 8dB, can still be effectively linearized by utilizing digital pre-distortion [4], [7].

In this respect, current industrial applications, utilize several new improved LDMOS bias temperature compensation circuits utilizing a discrete device small signal bipolar junction transistor network [8]. The characteristics of the mentioned

Antonis Constantinides is with the ET-Broadcast , Limassol, Cyprus (email: etbroadcast@hotmail.com).

⁴ Digital Video Broadcasting — Terrestrial it is the DVB

⁵ Orthogonal frequency-division multiplexing

⁶ B.E.R: Block Error Rate

device are used to reduce temperature drifting of the LDMOS in class A, AB single case-design amplifiers, where IDQ is ultra-critical. Temperature compensation in LDMOS amplifiers based on the fact that the quiescent current increases proportionally with the temperature enhancement of the LDMOS case (Tc) after reaching a certain temperature point. Therefore, temperature rate must be reversed and neutralized as described by Erickson's research engineer C. Blair in "Biasing LDMOS FETs for Linear Operation" [9].

However, according to our research, the mentioned discrete component bias temperature compensation circuit could enable a significant degree of error due to the different component tolerances. It is also very difficult to track and mirror the exact temperature rise due to the different thermal characteristics as well as operating conditions and topologies of the amplifier. For example, when two or more high power LDMOS constitute a single amplifier utilizing a common heat sink; heat dissipated by each device interacts to the others throughout the common heat sink.

II. MATERIALS AND METHODS

By incorporating a microprocessor controlled bias circuitry, we are targeting far more accurate results. Microprocessor operates as a control tracking system temperature compensator, designed to be used in topologies like Doherty, where two or more LDMOS semiconductors must be absolute temperature balanced or in any other applications where IDQ must be perfectly stable. The principle of the circuit is based on the voltage to temperature analog to digital and digital to analog conversation. It can be achieved by the use of an independent voltage source temperature sensing network that provides the temperature variations (-mV/C) of the LDMOS junction temperature (Tj) into a microprocessor controller. The choice of the microprocessor strictly depends on the compensation resolution requirements. As a result, the microprocessor can be programmed with the desired LDMOS thermal parameters in order to compensate accurately by creating the proper error voltage (VGS) at the gates of the device. The automatic temperature control block diagram is realized in Fig. 4.

Thermal dissipation is always in reverse proportionally to the amplifier's efficiency as well as proportional to the DC power dissipation of the LDMOS ratings. Thus, the choice of the LDMOS semiconductors which constitute the amplifier under test has been based on the thermal dissipation of its case (Tc), drain current operation (VDD), efficiency (η) as well as the cooling system employed. The methodology used is presented in Freescale's application note AN 2004 [10].

The power dissipation of the device can be expressed using (1):

$$Pdiss = (RF input power + DC power (ID * VD)) - (RF output power + RF reflected power) (1)$$

Junction - to-case thermal resistance is also calculated from (2):

$$\theta JC = (TJ - TC) / P dissipation$$
 (2)

As this research is in progress, a general overview of the amplifier's architecture is illustrated in Fig. 2. It forms a hardware system of interaction that presents the crucial key role parameters of efficiency, linearity, thermal stability, as well as bandwidth of a DVB-T signal amplifier.



Fig. 2 System of Interaction of a DVB-T Amplifier



Fig. 3 Automatic Temperature Control

The Automatic Temperature Control (Fig. 3) has been justified on a combined push pull LDMOS VHF (170-230MHz) DVB-T amplifier using two Freescale's [10] MRFE6VP61K25H. The amplifier has been mounted on a copper heat spreader plate with dimensions 20cm X10cmX0.5cm without applying forced-air cooling, so the temperature on the LDMOS's cases would rise very fast. The tested quiescent currents were set at 2A, 3A, 4A, 5A and the drain voltage at 50V. The drifting average response between 50-120C LDMOS operation without compensation is given in Fig. 4, whereas with compensation in Fig. 5.







Fig. 5 IDQ Versus Temperature with Compensation

III. CONCLUSIONS

Enhancing efficiency versus linearity has always been a major research trade off topic in UHF and microwave applications [11].

Temperature rise has forced many designers to settle the "back off" at a lower efficiency point in order to confirm that the linear amplifier will not drift operating from the linear region under excessive temperature conditions.

Our research has demonstrated that high power LDMOS disable reliable operation without employing a bias temperature compensation circuit even operating in class C.

According to our results, the quiescent current will have a great offset from the set value when the LDMOS will reach temperatures above 40C. Usually high power LDMOS will reach temperature levels up to 120C during long time operation.

Without compensation we detected a power output reduction up to 20% and gain instability.

Thus, achieving stabilization of the optimum efficiency will increase the average digital power of the transmitter as well as the efficiency.

The impact of energy consumption benefits also an entire network of transmitters becoming very friendly for the environment

It also creates new prospects for future research for the optimization of other crucial parameters like the matching network for higher return loss when "back off "is set at a very low power output point. Finally, it provides information to the semiconductor manufacturers to improve the performance of the new generation semiconductors based on new research evidence.

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